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Some developments in high-speed ferrite-core memories

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Table of Contents

Symbols Used

B	Flux Density
B_r	Remanent Flux Density
B_s	Saturation Flux Density
e_s	Output Voltage
H	Magnetic Field
H_c	Coercive Force
H_f	Full-flux Magnetic Field
H_o	Threshold Magnetic Field
I	Set Current
I_f	Full-flux Set Current
I_o	Threshold Set Current
I_B	Nominal Bit Current
I_R	Nominal Read Current
I_w	Nominal Write Current
I_{wt}	Nominal Total Write Current
I_o'	Set Current
I_f'	Set Current
k	Ratio of Minimum Write Current to Threshold Current
t_c	Cycle Time
t_R	Nominal Width of Read Pulse
t_w	Nominal Width of Write Pulse
t_d	Non-magnetic Delay Time
t_s	Characteristic Switching Time
t_p	Pulse Width

S_w	Switching Coefficients
T	Temperature
T_c	Curie Point (Temperature)
T_A	Ambient Temperature
X	Percentage of Flux Change
Φ	Partial Remanent Flux
Φ_r	Remanent Flux
Φ_s	Saturation Flux
R_s	Squareness Ratio

List of Figures

SOME DEVELOPMENTS IN HIGH-SPEED FERRITE-CORE MEMORIES

Abstract

The paper reviews some recent developments in high-speed ferrite core memories. A general discussion on the storage properties of ferrite cores and their switching characteristics is presented. Improvements in speed of operation of core memories by partial-flux switching are examined. A description of the 2D memory scheme is included. The effects of temperature on core characteristics, and on partial-flux switching are discussed. An attempt is made to present an approximate method for evaluating the cycle time of the 2D memory scheme. This is done by specifying the write and read current amplitudes, and then determining the switching times for the write and read periods, respectively. It is then shown that if the variations of percentage of flux switched, the threshold current, and the switching coefficient with temperature are assumed to be linear, the cycle time can be uniquely determined as a function of the core ambient temperature. Studies on relaxation effects of bit currents on core characteristics are briefly discussed. A new analytical technique which has been "proposed" for determining the cycle time of a 2D memory scheme as a function of core temperature is reviewed at the end.

SOME DEVELOPMENTS IN HIGH-SPEED FERRITE-CORE MEMORIES

1. Introduction

Ferrite cores have been investigated to study their switching characteristics as related to their use in fast memories. Recent methods have permitted a significant decrease in memory cycle time. One important method for decreasing the time and energy associated with the switching of the storage array cores has been accomplished by reducing the amount of flux change. This is attained by controlling the amplitude and width of the current driver supplying the magnetomotive force. The reversal of magnetization of a ferrite core requires a finite time to go to completion, the duration of this time being dependent upon the amplitude of the driving field, and the width of the current pulse. If the driving field is removed before the core has had time to completely switch into saturation, a partially switched state exists, and hence the name partial switching.

In ferrites, temperature is one important factor causing change in magnetization. From the basic theory of ferromagnetism[1,2], it is well known that the saturation magnetization of a ferrite material is temperature dependent. At

zero absolute temperature, a ferrite core would have its maximum magnetization. As the temperature is raised, the magnetization decreases, and at a temperature T_c, known as the Curie point, the ferrite core would lose its spontaneous magnetization, although it may have induced magnetization. A function relating the magnetization with the temperature of the core can be represented by a nonlinear curve.

Increasing the temperature of the surrounding environment of a ferrite core can thus change the percentage of flux which a given combination of current amplitude and pulse width can switch. Ferrite cores used in memory devices are subjected to wide temperature ranges, and they are usually designed to function at ambient temperatures that may range from 40 to 75°C. Consequently, the cycle times of ferrite core memory devices are temperature dependent.

It is the purpose of this review to discuss the switching characteristics of ferrite cores in general, and to describe the use of partial-flux switching in the design of high-speed core memories (with typical cycle times of the order of 500 ns to 200 ns). Temperature effects on the magnetic properties of ferrites, and on the operation of core memories are also discussed. An attempt will be made to present a simplified method for calculating the cycle time of one high-speed ferrite core memory (the 2D memory device), whose individual cores, due to repeated cycling, are heated above the ambient

temperature. A qualitative discussion on relaxation effects is also presented. A recent study made on the cycle time of a 2D core memory is examined at the end.

2. Ferrite Cores as Storage Elements

Ferrite cores widely used as storage elements in high-speed memories must exhibit rectangular or square magnetic hysteresis loops[3]. A typical "square" B-H loop, obtained by cycling the core between the limits $\pm H_f$ is shown in Fig. 1. It can be seen that the loop is almost flat-topped, and almost vertical-sided. The magnetic field H_f corresponds to the saturation flux Φ_s (or flux density B_s), and H_c is defined as the coercive force. The remanent flux is denoted by Φ_r, and B_r is the corresponding flux density. The degree of squareness of the B-H loop is significant, and a squareness ratio, R_s, is defined as the ratio, in hysteresis loop, of the flux difference between remanent states ($=2\Phi_r$) to the flux density difference between points of maximum applied magnetizing force ($=2\Phi_s$). Ferrite cores used as storage elements must have a very large squareness ratio.

The storage properties of ferrite cores also depend on there being two distinct states of a remanent flux[4]. The flux is normally at the position marked "O" (or $-\Phi_r$). If the applied field is less than H_o (see Fig. 1), there will be no significant change in flux. Normally H_o is less than

H_c, and it is defined as the threshold field. If the applied field is equal to or greater than H_o, there will occur an irreversible flux change. For $H_o \leq H < H_f$, the flux will be switched from $-\Phi_r$ to Φ, where Φ is less than $+\Phi_r$. Under such conditions, the ferrite core is operated on a minor hysteresis loop, and the flux change is referred to as partial switching. For $H \geq H_f$, the full area of the major loop is employed, and the two states of the binary digit are stored as $-\Phi_r$ and $+\Phi_r$. When partial switching is employed, $-\Phi_r$ is referred to the nominal "0" state, and Φ is referred to as the nominal "1" state.

Another representation of the binary states of a ferrite core is the so-called "S" curve shown in Fig. 2. In the "S" curve representation, the percentage of flux change X ($= \Phi/2\Phi_r \times 100\%$) is plotted against the magnetizing field H. Depending on the magnitude of the magnetizing field, X is about 50% if the minor loop goes from $-\Phi_r$ ("0" state) to =0 ("1" state) with H equal to H_c. X will be 100% for the major loop ($H \geq H_f$). By controlling the duration of the magnetizing field (or current), it is possible to have many "S" curves. This will be seen after an examination of the switching characteristics of ferrite cores.

3. Ferrite Core Switching Characteristics

A very convenient method for determining the switching characteristics of a ferrite core is to study its response to a current pulse of constant amplitude. The basic arrangement for such a test is shown in Fig. 3. A single-turn input wire carries a step current with a fast rise time, and with an amplitude at least equal to I_f, where I_f is the magnetizing current that would correspond to H_f (see Fig. 1). Suppose the initial remanent flux is $-\Phi_r$ ("0" binary state), then the core will be switched to $+\Phi_r$ ("1" binary state) when the current I is applied. Fig. 4(a) shows a typical output voltage waveform across an output single winding. This induced voltage is equal to the rate of change in flux $d\Phi/dt$. If the core had initially been set at $+\Phi_r$, the output voltage waveform would be similar to the one shown in Fig. 4(b). Because the flux is changing from $+\Phi_r$ to $+\Phi_s$, the amplitude of the induced voltage shown in Fig. 4(b) is very small compared to that shown in Fig. 4(a).

The reversal of magnetization will take a finite time to go to completion. Switching around the major loop from $-\Phi_r$ to $+\Phi_r$, the ferrite core takes a characteristic switching time, t_s, which is defined as the time at which the voltage e_s (see Fig. 4(a)) has fallen to 10% of its peak value. It has been shown, both experimentally and theoretically[5],

that the switching time, t_s, is related to the driving current I by the approximate relation

$$t_s = \frac{S_w}{I - I_o} \qquad (1)$$

where I_o is the threshold current (corresponding to H_o), and S_w is defined as the switching coefficient. In practice, it has been found more convenient to study the inverse switching time (also called switching speed), $1/t_s$, as a function of I or H. Thus S_w will be equal to the inverse slope of the $1/t_s$ versus I curve. Such a curve, known as the switching curve, is shown in Fig. 5. Eq. (1) predicts a linear relationship between the inverse-switching time and the applied field. Experimental switching curves (which are similar to the one shown in Fig. 5), however, exhibit three regions having different values of switching coefficients. A three-mechanism model has been proposed to explain the flux reversal process in each region[6]. In the low-drive region (region I), the flux reversal is attributed to the motion of domain walls. In the intermediate-drive region (regionII), the flux reversal is faster, and it is assumed to be due to non-uniform rotation of domains. For fields above H_2, a third high-drive region exists in which the flux reversal is believed to be due to uniform rotation of domains.

The empirical linear relationship between the switching speed and the driving field predicted by Eq. (1) is approximated to a good degree in the low-drive region. Since the

curves in the intermediate and high-drive regions are also straight lines, it has been shown that Eq. (1) can be modified for use at the higher fields[7]. For applied fields between H_1 and H_2, Eq. (1) becomes

$$t_s = \frac{S_w S_1}{S_1 (H_1 - H_o) \quad S_w (H - H_1)} \qquad (2)$$

and for applied fields above H_2, the switching time is given by

$$t_s = \frac{S_w S_1 S_2}{S_1 S_2 (H_1 - H_o) + S_2 S_w (H_2 - H_1) + S_o S_1 (H - H_2)} \qquad (3)$$

where S_w, S_1, and S_2 are the switching coefficients for fields greater than H_o, H_1, and H_2, respectively.

Instead of measuring t_s, some workers measure t_ϕ, the time at which 90% of the reversible flux has switched. Determination of the latter involves the integration of the output voltage. The time, t_{pk}, at which the output voltage e_s takes its peak value, is also sometimes measured.

4. Partial-Switching Characteristics of Ferrite Cores

In region I of Fig. 5, where values of the driving field H vary from H_o ($\leq H_c$) up to H_1 ($< H_f$), the core can be operated on a minor hysteresis loop - i.e., the core flux

can be partially switched. In storage applications, the percentage of flux switched when a ferrite core changes from the nominal "1" to the nominal "0" state is normally less than 80 percent[8]. This causes a reduction in the switching time when the cores are driven from various values of remanent flux to the "0" state. Fig. 6(b) shows the voltage outputs obtained by applying a constant amplitude driving field to a core which has been previously set to various remanent states A to D in Fig. 6(a). It can be seen that considerably lower switching times are obtained from a partially switched core than from one which is switched from $+\Phi_r$ to $-\Phi_r$.

The time taken for a core to switch from one state to another is a function of the amplitude of the feild [9, 10]. In general, the more the driving force that is available, the faster will the core switch. This is illustrated by the family of curves shown in Fig. 7, where both the switching speed (or inverse switching time) and the driving field have been normalized. It can be seen that the switching speed is directly proportional to the driving field that is applied. It should also be recognized that the switching speed is faster when partial-flux switching is employed.

The amount of flux switched also depends on the duration of the driving field [11]. Fig. 8 shows a family of "S" curves in which the percentage of flux change, X, is plotted against the driving field with pulse width, t_p, as a parameter. It

can be noted that pulses very much larger in amplitude than the threshold field may be repeatedly applied to a core in the "0" state without causing any appreciable change of flux, provided that the pulses are of very short duration compared to the characteristic switching time of the core. This important property is useful in evaluating ferrite cores for fast memory devices in which partial-flux switching is employed.

5. The 2D Memory Device

One basic technique in which ferrite cores can be arranged to form a storage system is known as the "word-organized" or "linear-selection" scheme. In this system, small ferrite cores with square hysteresis loops are arranged in a rectangular array or matrix. The cores can be switched from one remanent state to another using two or more wires passing through each core with current in any wire. The 2D (2 "dimensional") memory is one such scheme with two wires passing through each core, and with the possibility of passing current through either wire. The array, which is illustrated in Fig. 9, is organized with the word lines situated horizontally, and bit lines situated vertically. To switch a core from the "0" state to the "1" state, a write-current pulse of amplitude I_w is impressed on the X-wire passing

through the core; at the same time a bit-current pulse of amplitude I_B is impressed on the Y-wire passing through the core. Normally, I_w is approximately equal to I_o (threshold current), but I_B is less than I_o. The coincidence of these two pulses provides a total switching current I_{wt} which causes a "1" to be written in that core which receives both the write and bit currents. If it is desired to write "0" in a given binary word, it can be done by sending zero I_B in the corresponding Y-wire. For example, in writing the word 1101, the bit current in Y_3 is zero. Since I_w is approximately equal to I_o, the write current alone will cause no appreciable change in flux. That is to say, the amount of flux switched by the write current alone can be considered to be reversible, while the amount of flux switched by the total sum of write (I_w) and bit (I_B) currents is irreversible. Thus the direction of the bit current (Fig. 9) is chosen to assist the magnetizing action of the write current.

The written binary word is read by sending a read current, I_R, through the X-wires, but in opposite sense to the write current direction. The read current, I_R, must have sufficient amplitude and duration to switch the core completely to a stable reference "0" state ($-\Phi_r$), whether it was previously in the $+\Phi_r$ state or any other nomianl "1" state. The reading process of the 2D memory device is known as DRO (destructive read out). After the current I_R is passed, the stored

information is destroyed. Thus a "write" (or "rewrite") period follows a "read" period. Switching is toward the "1" state during write, and toward the "0" state during read out. The read-wire outputs are shown in Fig. 10, which are similar to the waveforms illustrated in Fig. 4. Waveform "1" would indicate that the initial binary state was "1"; waveform "0" would indicate that the initial binary state was"0".

A simplified timing diagram of the 2D memory scheme is shown in Fig. 11. The cycle time, t_c, can be defined as the time required to write a bit of information into, and then read out of the memory, plus a non-magnetic delay-time. The read current flows for time t_R. This is followed by a pause, t_1, at the end of which the write current is established. The write pulse has a duration t_w, and it is followed by another pause t_2, during which both the write current and the read current are zero. The cycle begins again at the end of t_2. The duration of the bit pulse is smaller than t_w. If we let t_d (the non-magnetic delay time) be equal to the sum of t_1 and t_2, then we have the expression for the cycle time given by

$$t_c = t_R + t_w + t_d \qquad (4)$$

Partial-flux switching is employed in the 2D memory device. The amplitude of the total write current, I_{wt}, is then limited by selection requirements. Its duration, t_w, is also smaller than the characterisitc time, t_s,

of the core. To stablize the "0" state, the amplitude of the read current is made larger than the total write current amplitude. This will also shorten the duration of t_R. Typically, if $t_w = t_s$, and $t_R = t_s/2$, then the minimum cycle time would be approximately $3t_s/2$. Because of numerous sequential curcuit delays and the driving currents rise and fall times, it is difficult to make t_d equal to zero. But it can be assumed that t_d can have a maximum value equal to the sum of t_R and t_w. With this approximation, the cycle time will have a total duration of $3t_s$. It has been pointed out[12] that in practice it is difficult to achieve a cycle time of less than $4t_s$. This is because of numerous sequential circuit delays and the rise and fall times of the driving currents.

There is also another serious limitation to the switching speed of ferrite core memories (including the 2D memory), and that is the deterioration of magnetic properties of heated cores due to repeated cycling of the read-write currents. A review of temperature effects on the ferro-magnetic properties of ferrites is presented in the following section. The effects of temperature on partial-flux switching are also briefly discussed.

6. Effects of Temperature

6.1 Temperature Effects on the Hysteresis Loop of a Ferrite Core

The temperature dependence of the magnetic properties of

ferrite cores can be deduced from the theory of ferromagnetism. Typically, the saturation flux, Φ_s, of a ferrite core decreases with temperature (Fig. 12) until it essentially disappears at the Curie point, T_c. At lower temperatures remote from the Curie point, the change in Φ_s is small and is relatively linear with temperature. Ferrites with a higher coercivity have a higher Curie point[13]. In general, as the temperature of a ferrite core increases, the following effects are observed.

(i) The coercive force, H_c, is reduced; the variation of the threshold field, H_o, is also parallel to that of H_c (Fig. 13)

(ii) The flux density decreases.

(iii) The slope of the relatively flat portions of the hysteresis loop becomes more pronounced.

Thus a heated core tends to switch faster. The voltage output from a heated core is also temperature dependent. Consequently, temperature coefficients must be included in the specifications of ferrite core memories. One important property which must be specified is that the ferrite cores must possess low temperature coefficients of coercivity. It has been reported that the rate of decrease of H_c (and H_o) is usually slightly in excess of one-half percent per degree centigrade[14].

6.2. Temperature Effects on Partial-Flux Switching

When a word is continuously cycled at high frequencies (100 kc/s to 2 mc/s or even higher), the power dissipated in partially switched cores can result in a large increase in core

temperature and degradation of the core characteristics. A partially-switched state is more sensitive to temperature effects than a fully-switched state[15]. Relatively small changes of the temperature of a partially-switched ferrite core will introduce large changes of the amount of flux that is switched. Fig. 14 shows the variation of flux switched over a 6:1 range of temperature, plotted as a percentage of the flux value measured at room temperature (20°C). If the flux switched at room temperature is Φ, the flux available for switching at 120°C will be approximately 80 percent of Φ. The switching coefficient, S_w, also decreases as the temperature of the core is increased[16]. This effect is illustrated in Fig. 15, where the variation of S_w with temperature is assumed to be linear. With reference to Eq. (1), it can be noted that a decrease in S_w also means a decrease in the switching time, t_s.

7. An Approximate Method of Evaluating the Cycle Time of 2D Memory Schemes

It appears that it is possible to evaluate the cycle time of 2D memories by determining the switching times for the writing and reading process using equation (1). If the amplitude of the write current is specified, and the final flux value of the nominal "1" state (or the percentage of flux change) is also known, the duration of the write pulse can be determined by setting it equal to the switching time during

the writing process. Similarly, the duration of the read pulse can also be set equal to the switching time during the reading process. The cycle time of the memory will then be approximated by the sum of the switching times during the write and read periods plus a delay time.

Since the switching coefficient (S_w), the threshold current (I_o), the full-flux switching current (I_f) and the percentage of flux change (X) are all temperature dependent, it is necessary to know the ambient temperature of the ferrite cores and their specific heat coefficient. Dimensions of the cores in the 2D memory must also be specified. Ferrite cores used in the 2D memory are of small dimensions (typically, the inner diameter may be as small as 10 mils); they must possess rectangular hysteresis loops. They must have low specific heat coefficients, allowing operation of the memories at an ambient temperature that may range from 40°C up to 75°C, or even higher. The variations of the parameters I_o, I_f, X and S_w with temperature can be assumed to be linear. In the design of ferrite core memories, it is also generally necessary to operate on one of a family of minor hysteresis loops (see Fig. 1 and Fig. 2) in which partial flux switching is employed. The percentage of flux change (X) is normally less than 80 percent.

We consider a linearized "S" curve (Fig. 16) in which the actual curve is approximated by a straight line. It must be noted that the threshold field is increased from I_o to I_o'. On the other hand, the full-flux switching current I_f' given by the linear curve is smaller than the actual I_f. The percentage of flux change will be also affected--a high value of X on the linearized curve would correspond to a smaller value on the actual "S" curve.

The minimum allowable total write current must irreversibly switch a core from X = 0 to X_{min}. This is given by

$$I_{wt} = I_o' + X_{min} (I_f' - I_o') \tag{5}$$

in which the wirte current is given by

$$I_w = I_o' \tag{6}$$

and the bit current is given by

$$I_B = X_{min} (I_f' - I_o') \tag{7}$$

Normally, the write current makes 60 percent of the total write current, and the remaining 40 percent is made up by the bit current. If we define the ratio of I_{wt} to I_o' by k, the following condition must be satisfied:

$$\frac{I_{wt}}{I_o'} = k \qquad (1 < k < 2) \tag{8}$$

and thus

$$I_B = X_{min}(I_f' - I_o')$$

$$= (k-1)I_o' \tag{9}$$

which is less than I_o', because the constant k is less than 2 as indicated in E_q. (8).

The switching time for the writing process will be

$$t_w = \frac{S_w}{I_{wt} - I_o'}$$

$$= \frac{S_w}{X_{min}(I_f' - I_o')} \tag{10}$$

where S_w is the switching coefficient.

The read current must have a larger amplitude than I_{wt} so that its duration is shorter than t_w. We arbitrarily set

$$\frac{I_R}{I_o'} = (k+1) \tag{11}$$

where k is defined in E_q. 8. Thus,

$$I_R = 2I_o' + X_{min}(I_f' - I_o') \tag{12}$$

Therefore, the switching time for the read process will be

$$t_R = \frac{S_w}{I_R - I_o'}$$

$$= \frac{S_w}{I_o' + X_{min}\,(I_f' - I_o')} \tag{13}$$

It can be assumed that the delay time, t_d, will not exceed t_w. Thus the total cycle time for the 2D memory scheme can be approximated by

$$t_c = \frac{2S_w}{X_{min}\,(I_f' - I_o')} + \frac{S_w}{I_o' + X_{min}\,(I_f' - I_o')} \tag{14}$$

With reference to the discussion on temperature effects, we have assumed that the temperature variations of the parameters X, I_o', I_f' and S_w are linear. Thus we can set the following experessions:

$$S_w = a_1 T + b_1 \tag{15}$$

$$X_{min} = a_2 T + b_2 \tag{16}$$

$$I_o' = a_3 T + b_3 \tag{17}$$

$$I_f' = a_4 T + b_4 \tag{18}$$

where T is temperature, and the coefficients a_1, a_2, a_3, a_4, and the constant parameters b_1, b_2, b_3, b_4 are to be determined from experimental curves. If these coefficients and constant parameters are known, the cycle time, t_c, given by Eq. (14) can be uniquely expressed as a function of temperature.

The temperature, T, in Eqs. (15), (16), (17) and (18) is the ambient temperature, T_A, plus a small temperature difference, Δ. A further simplification can be made by assuming that Δ is too small in comparison with T_A. This would still make the method presented above highly simplified. The approximations can be justified, however, by the fact that the cores in the 2D memory (as in most other core memories) are operated at a temperature far lower than the Curie point, where the influence of temperature is greatest. It would be interesting to know if the method outlined above could have any usefulness at all.

8. Recent Studies in High-Speed Ferrite Core Memories

The basic principles behind the operation of high-speed ferrite core memories (with particular reference to the 2D memory device) have been surveyed. The purpose of the following discussion is to examine two recent studies which have been made on problems associated with partial flux switching and temperature effects on the operation of core memories. Problems which are related to the relative instability of the partially switched state have been investigated. These problems which are generally referred to as relaxation effects are briefly examined in section 8.1. Over the past few years, new empirical techniques and mathematical formulations have been introduced to obtain high-speed cycle

time operation of core memories over wide temperature ranges. A complete mathematical theory which has been "proposed" to determine an optimum speed for the operation of a 2D memory as a function of core temperature is reveiwed in section 8.2.

8.1. Relaxation Effects[17]

One very important property of a memory core is that the repeated application of a drive current less than I_o will have negligible permanent effect on a core in either the nominal "1" or nominal "0" state. Thus in the 2D memory, the effect of the bit current alone on a partially switched state should be negligible. One difficulty arises, however, due to the relative instability of the partially switched state. When a core is disturbed by a bit current alone, and then the bit current is removed, part of the flux will revert to its initial value with a time constant. The relaxation time is reported to depend on the amplitude of I_B and its duration. When the reading process follows the write phase, the signal caused by relaxation in the unselected cores may be comparable during read-out time with the signal from the selected cores. There is also the possibility of a gradual shift of the minor hysteresis loop over many cycles of operation, with a resulting variation in output signal. Thus a core in a partially switched

state is more sensitive to disturbing current less than or equal to I_o, and this imposes limitations on the selection matrix. In practice, relaxation effects have been assumed to be negligible in the calculation of cycle times.

8. 2. An Analytical Study of 2D Memory Cycle Times [18]

Recently, a complete mathematical theory has been "proposed" to determine the cycle time for the 2D memory. In this new analytical technique, the remanent flux and the threshold field are taken as quadratic functions of temperature. It is shown that if the core temperature is known, specifying either the amplitude or the duration of the pulse will uniquely determine the remaining term. It is also indicated that knowing the inner and outer diameters of the ferrite cores, the ambient temperature, the amplitudes of driving fields (as functions of temperature) and the percentage of flux change, it is possible to calculate the optimum pulse width that would minimize the cycle time. Quite a large number of unknown parameters, and error factors for the pulse width have been introduced into the various equations. The only difficulty with this technique is that the algebraic equations become too unmanageable, and the use of a computer is necessary for determining the parameter and tolerance factors. On the other hand, this technique is the only complete mathematical theory that has been formulated

for this type of operation so far. It has been pointed out that the technique could be explored to correlate costs of production and optimum speed of operation.

9. Summary

Ferrite cores used as storage elements in high-speed core memories must generally exhibit square magnetic hysteresis loops. Their storage properties depend on there being two distinct states of a remanent flux. The $-\Phi_r$ state is labelled as the nominal "0" state. If full-flux switching is employed, the $+\Phi_r$ state is referred to as the nominal "1" state. If partial-flux switching is employed, a flux state Φ less than $+\Phi_r$ is labelled as the nominal "1" state. To effect an irreversible flux change, it is necessary to apply a magnetizing field equal to or greater than the threshold field H_o. Normally, H_o is less than the coercive field H_c.

For switching around the major loop from $-\Phi_r$ to $+\Phi_r$, the core material has a characteristic switching time t_s, which is inversely proportional to the difference between the driving field and the threshold field. The switching time decreases when partial-flux switching is employed, i.e., when the core is switched from Φ (less than $+\Phi_r$) to $-\Phi_r$, or vice versa. Conversely, for a given driving field, the flux

switched from one state to another varies with the duration of the driving field.

Small cores are utilized in high-speed ferrite core memories. To improve the switching speed, and consequently to shorten the cycle time of operation, partial-flux switching is employed. This also reduces the power required to drive an array of storage elements. The minimized core size, the partial-flux switching, and the low-power consumption have advantages for high-speed operation (typical cycle times are of the order of 500 ns to 200 ns). One example of a high-speed core memory is the 2D (two dimensional) scheme. In this scheme, ferrite cores are arranged in a rectangular array of matrix. Two wires, one horizontal (called word-wire), and one vertical (called bit-wire), pass through each core. To switch a core from the nominal "0" state to the nominal "1" state, a write-current is impressed through the word-wire. At the same time, a bit-current is impressed through the bit-wire. Normally, the write current is approximately equal to the threshold current, I_o, but the bit current is less than I_o. The coincidence of the write and bit current provides a total write current which causes a "1" to be written in that core which received both the write and bit currents. Reading out of information (switching from "1" to "0") is accomplished by sending a read current through the word-wires, but in opposite sense to the write current direction. The reading process of the 2D memory

device is known as DRO (destructive read out). After the read current is passed, the information is destroyed, and thus a "read" period is followed by a "write" period. The cycle time of the 2D memory is given by the sum of the durations of the read and write current pulses, plus a nonmagnetic delay time.

From the basic theory of ferromagnetism, it is known that an increase in the temperature of ferrites causes a degradation of the core characteristics. The partial-flux switching technique is very sensitive to temperature changes. When a core is continuously cycled at a high frequency, the power dissipated in the cores gives rise to a large increase in core temperature. Experimental data indicate that the flux switched, the threshold field, and the switching coefficient decrease with an increase of core temperature.

It can be assumed that, within a limited range of temperature far below the Curie point, the variations of the important parameters with temperature are linear. With these approximations, and specifying the write and read current amplitudes, the cycle time of a 2D memory scheme might be evaluated by determining the switching times for the write and read processes, respectively. It must be pointed out, however, that this approach is highly simplified, and it would be interesting to know if it could have any usefulness at all.

Studies have been made on the influence of relaxation effects on partial-flux switching technique. When a core in the partially switched state is disturbed by a write current, then, when the write current is removed, part of the flux will revert to its initial value with a time-constant effect. There is also the possibility of a gradual shift of the minor hysteresis loop over many cycles of operation, with a resulting variation in output signal.

A new mathematical theory has been "proposed" recently to determine the optimum cycle time for the operation of the 2D memory scheme. In this analytical technique, the remanent flux and the threshold field are taken as quadratic functions of temperature. It is shown that if the core temperature is known, specifying the amplitude of the driving pulse will uniquely determine its duration. It is then shown that if the inner and outer diameter of the ferrite cores are also known, it is possible to calculate the optimum pulse widths that would minimize the cycle time of the memory. It has been pointed out that the technique could be explored to correlate costs of production and optimum speed of operation.

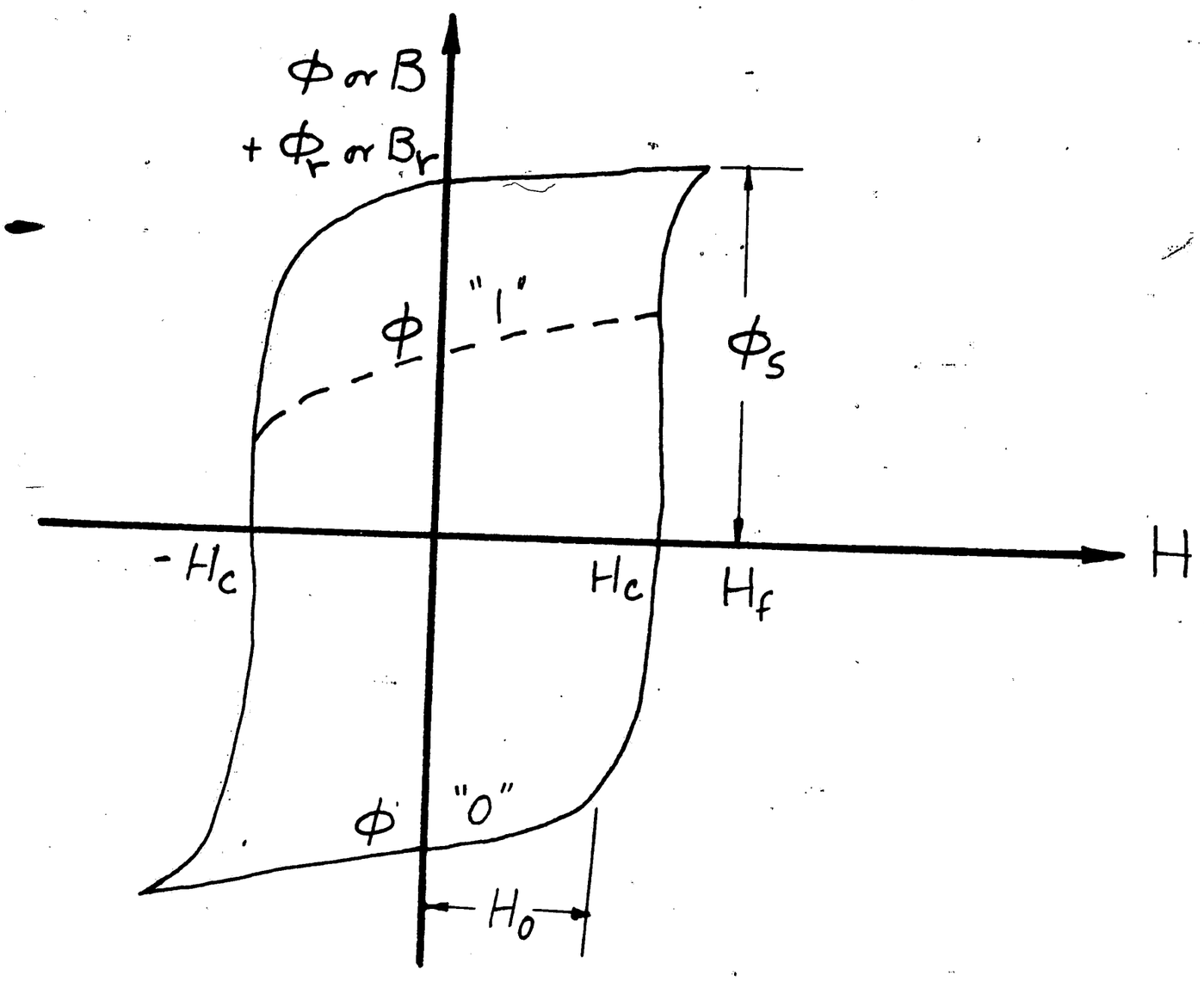

FIG. 1 - RECTANGULAR HYSTERESIS LOOP

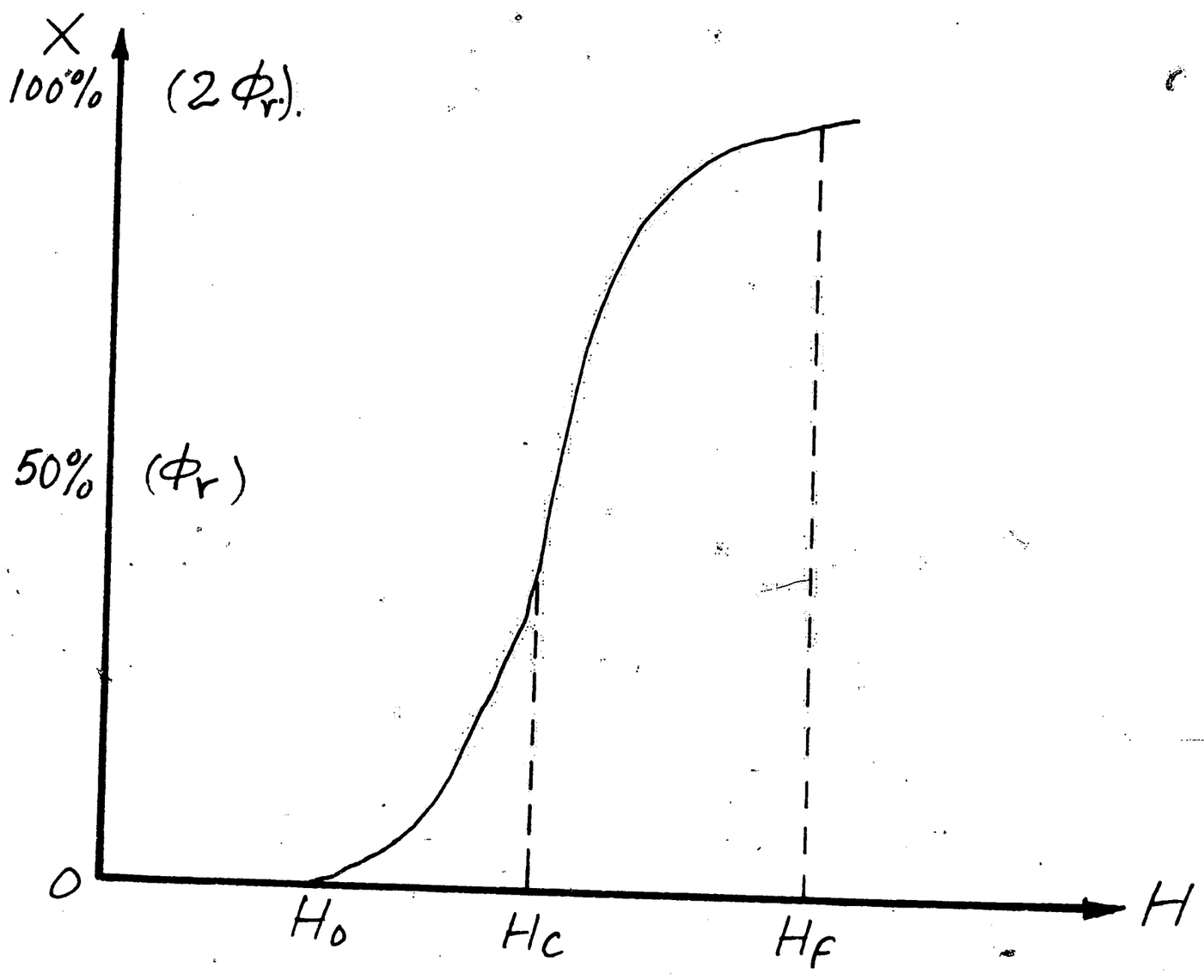

FIG. 2 - "S" CURVE

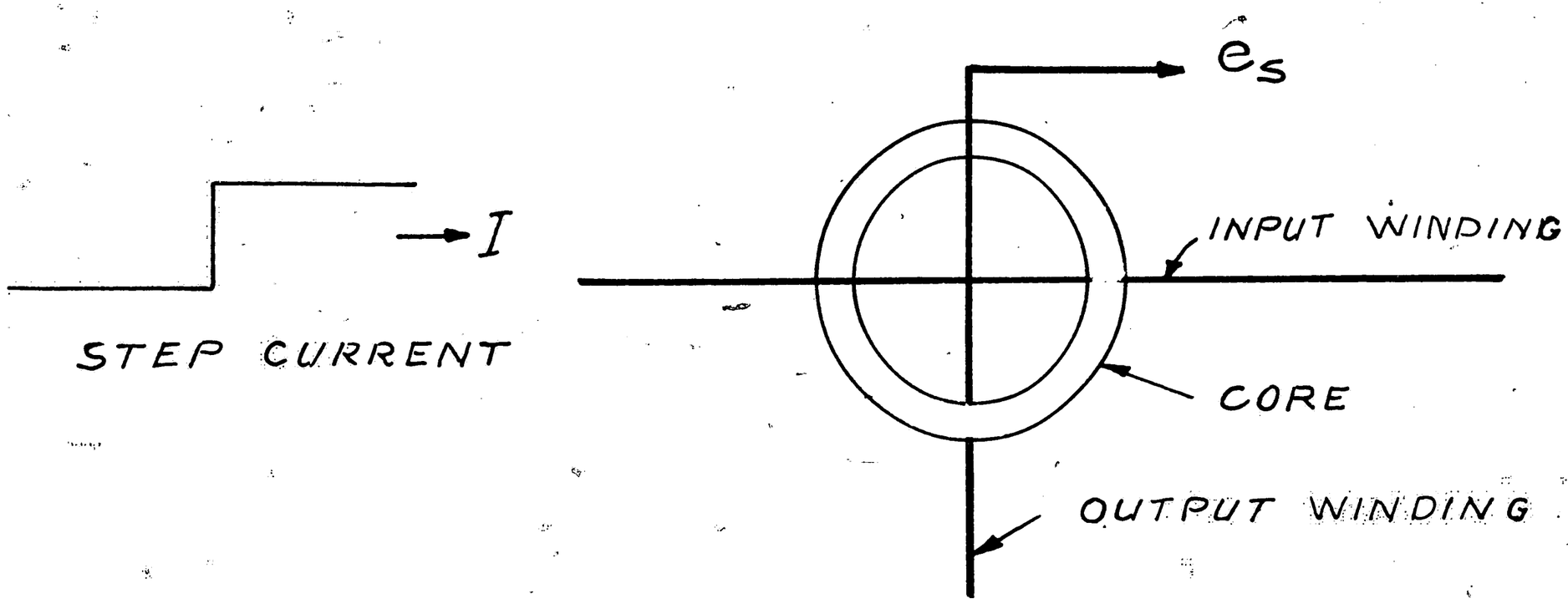

FIG. 3 - BASIC CORE TEST

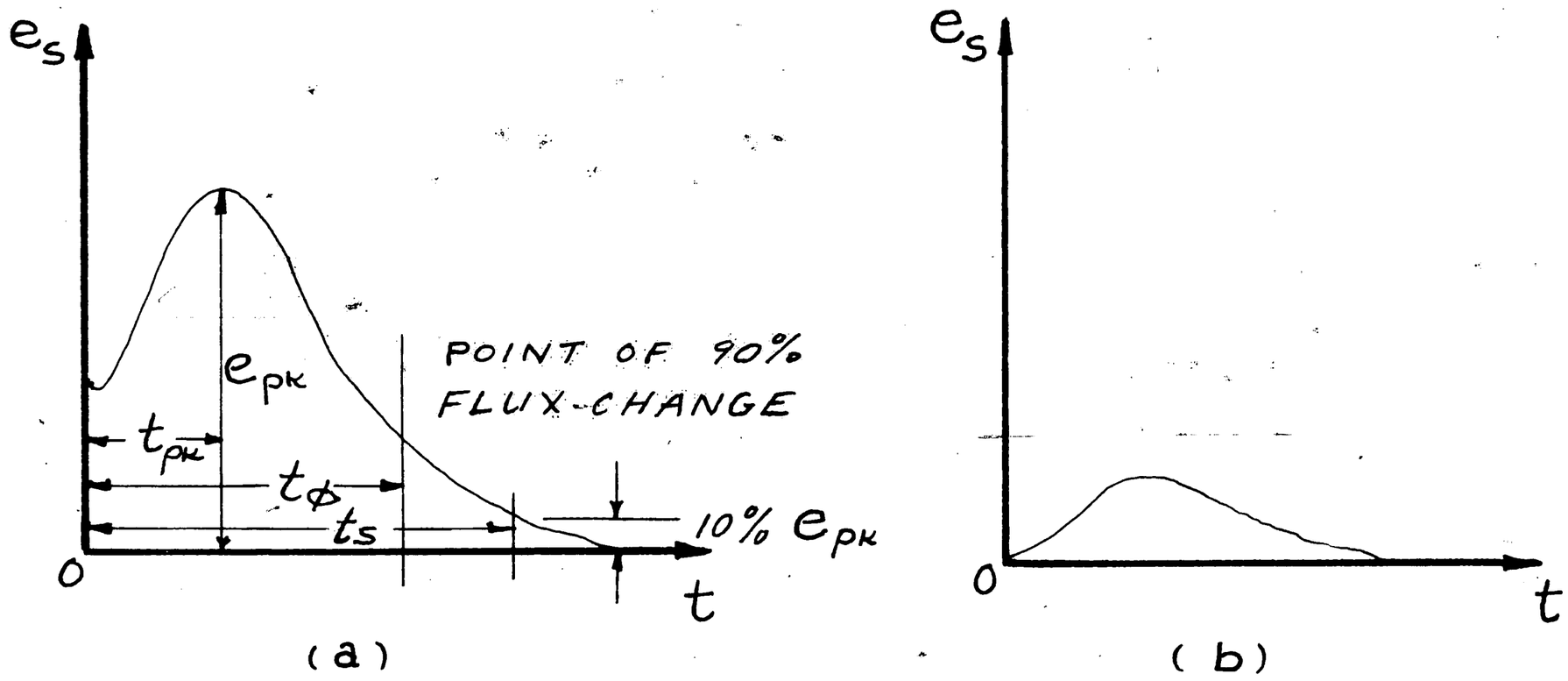

FIG. 4 - TYPICAL CORE OUTPUT VOLTAGE WAVEFORMS
(a) - CORE SWITCHING FROM $-\phi_r$ TO $+\phi_r$
(b) - CORE SWITCHING FROM $+\phi_r$ TO ϕ_s (or $-\phi_r$ to $-\phi_s$)

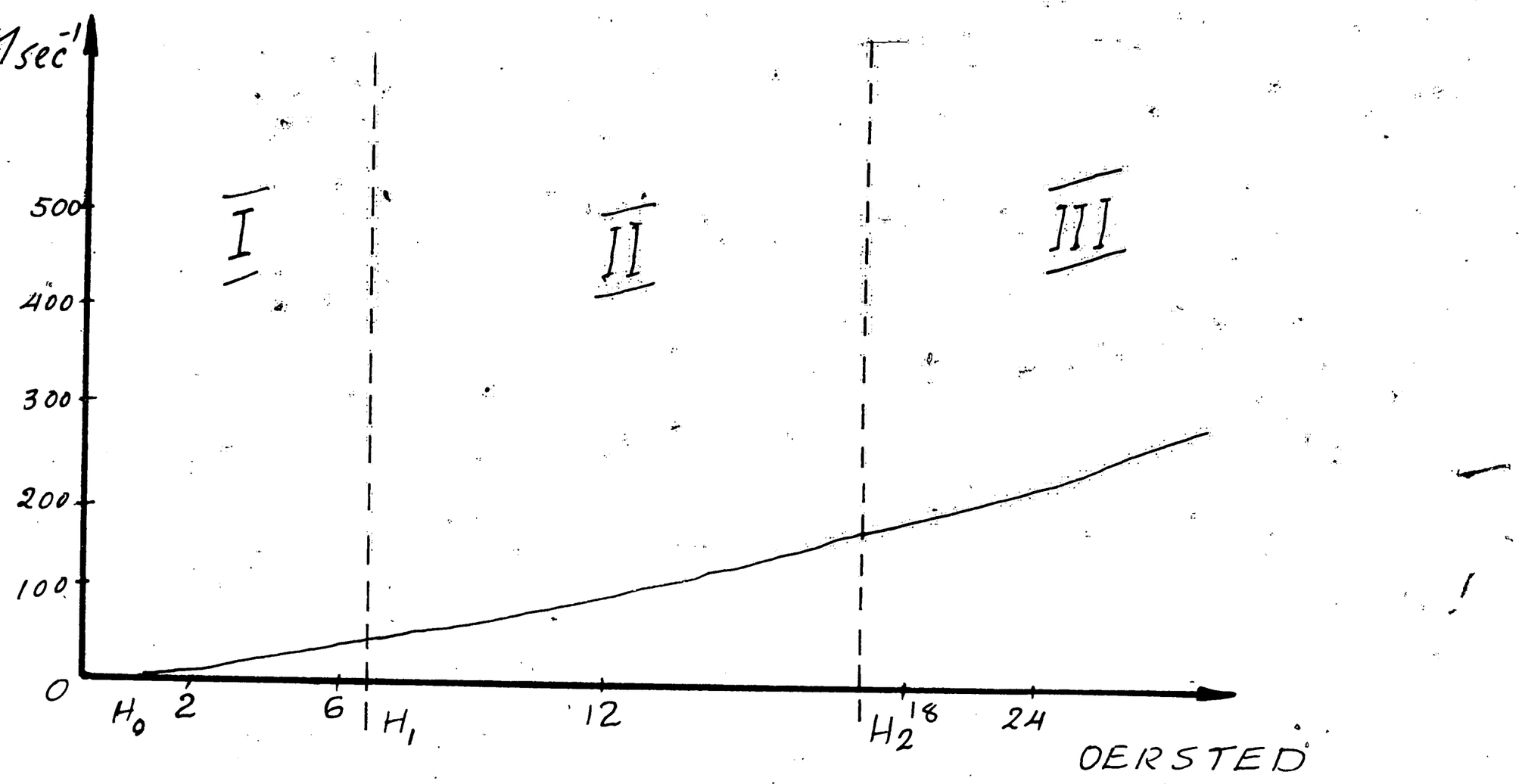

FIG. 5 - SWITCHING SPEED ($1/t_s$) VS. SWITCHING FIELD

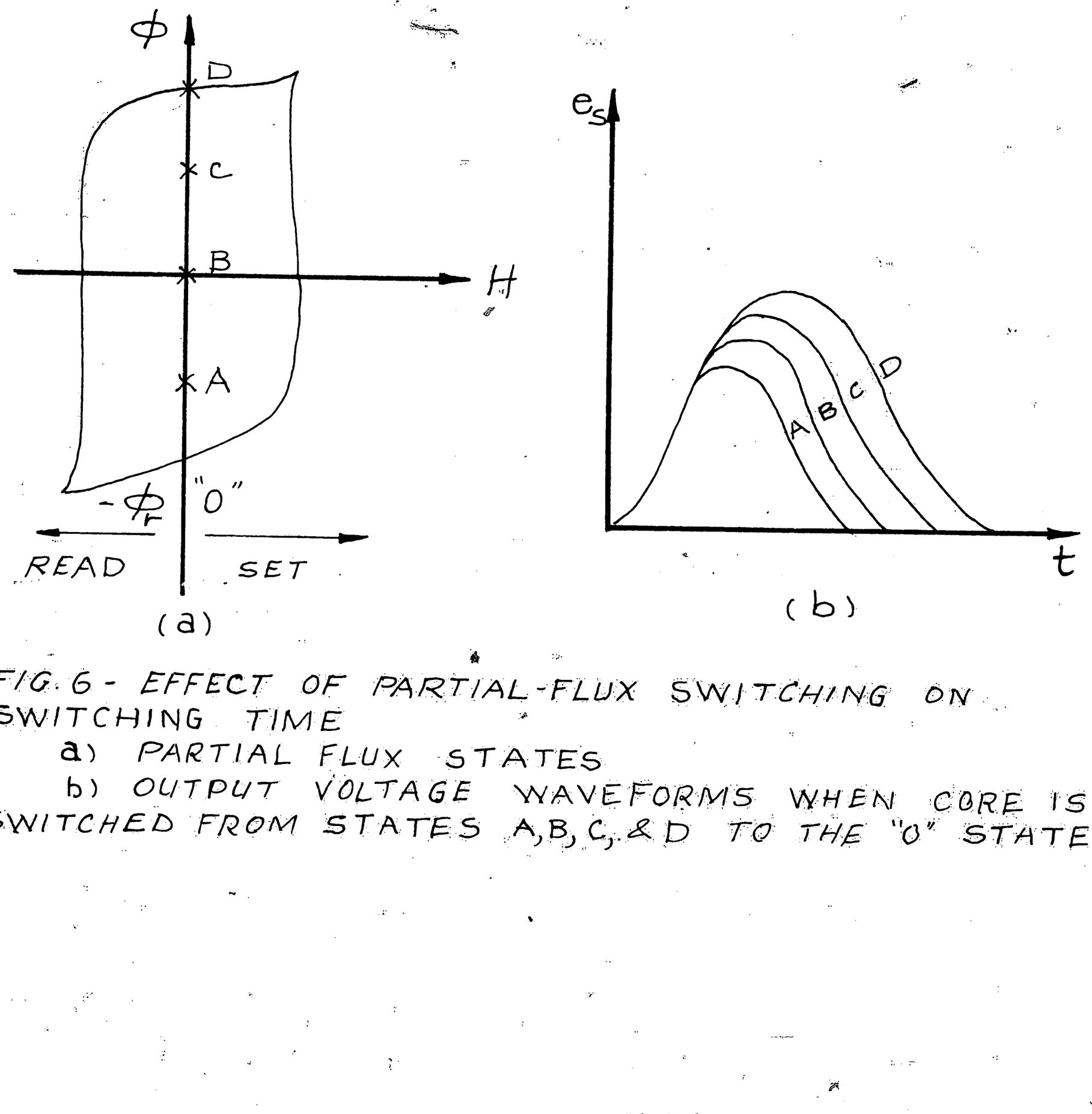

FIG. 6 - EFFECT OF PARTIAL-FLUX SWITCHING ON SWITCHING TIME
a) PARTIAL FLUX STATES
b) OUTPUT VOLTAGE WAVEFORMS WHEN CORE IS SWITCHED FROM STATES A, B, C, & D TO THE "0" STATE.

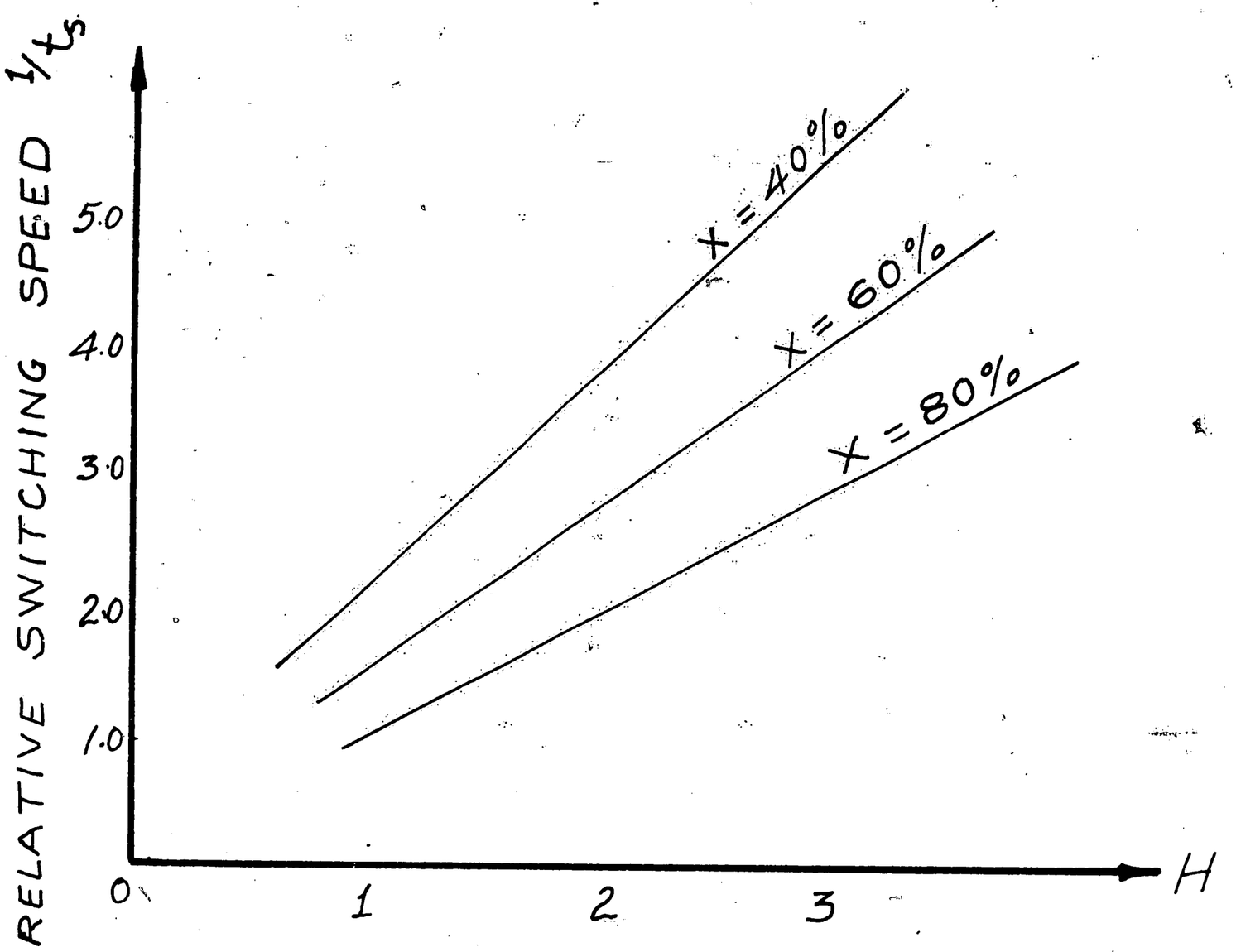

FIG. 7 - PARTIAL FLUX SWITCHING CHARACTERISTICS

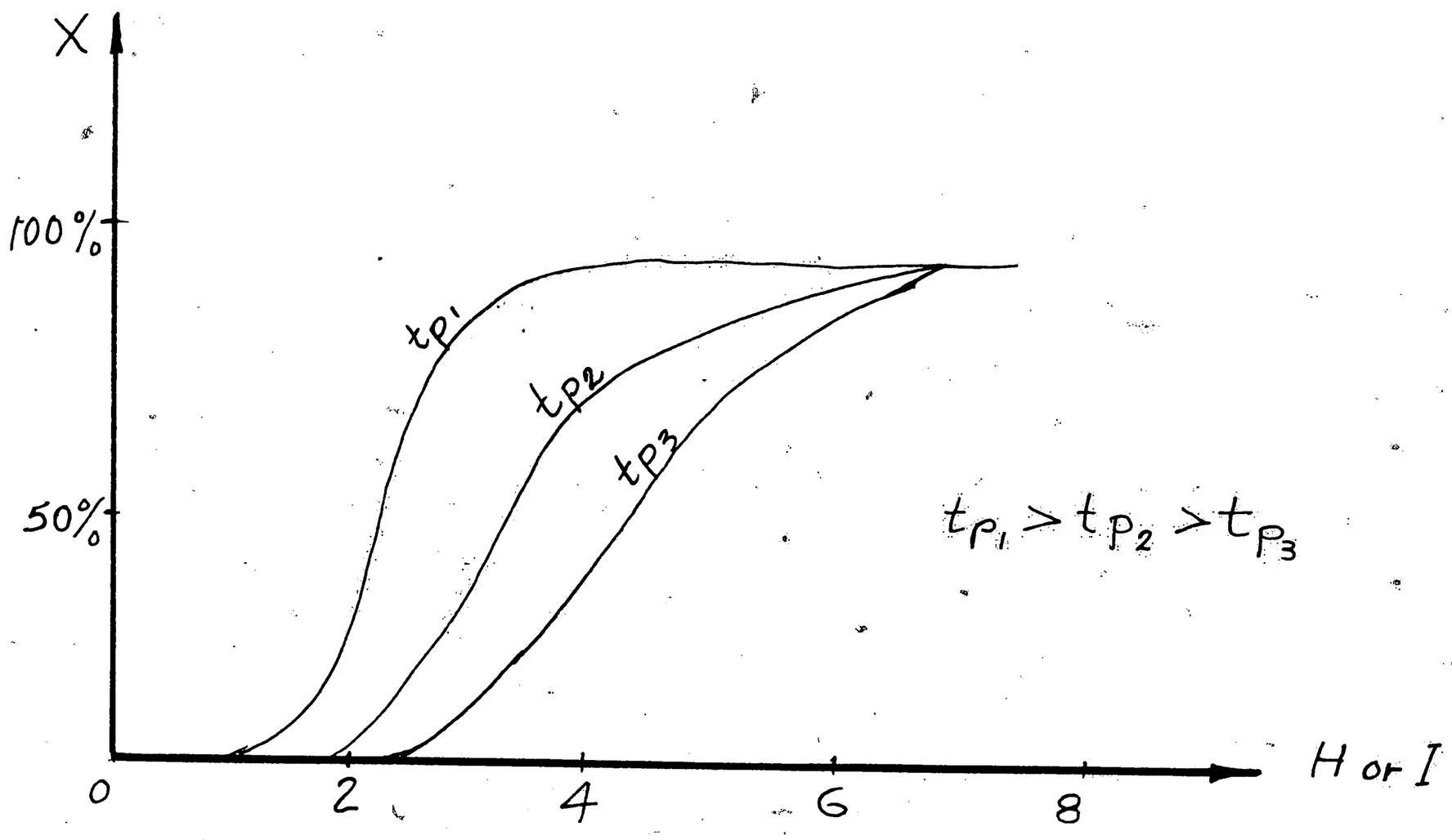

FIG. 8 - EFFECT OF PULSE WIDTH ON PARTIAL-FLUX SWITCHING

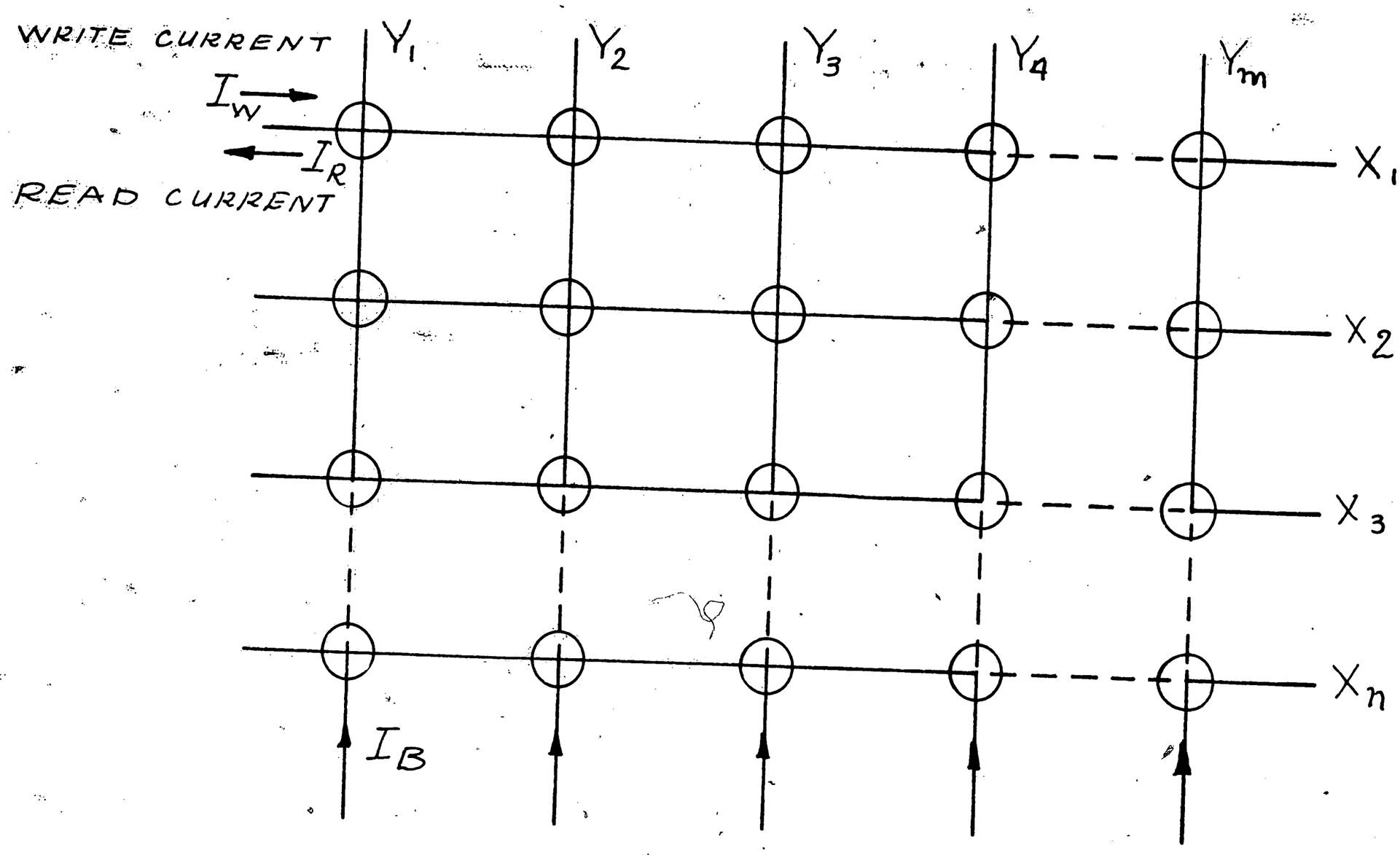

FIG. 9 - 2D MEMORY MATRIX

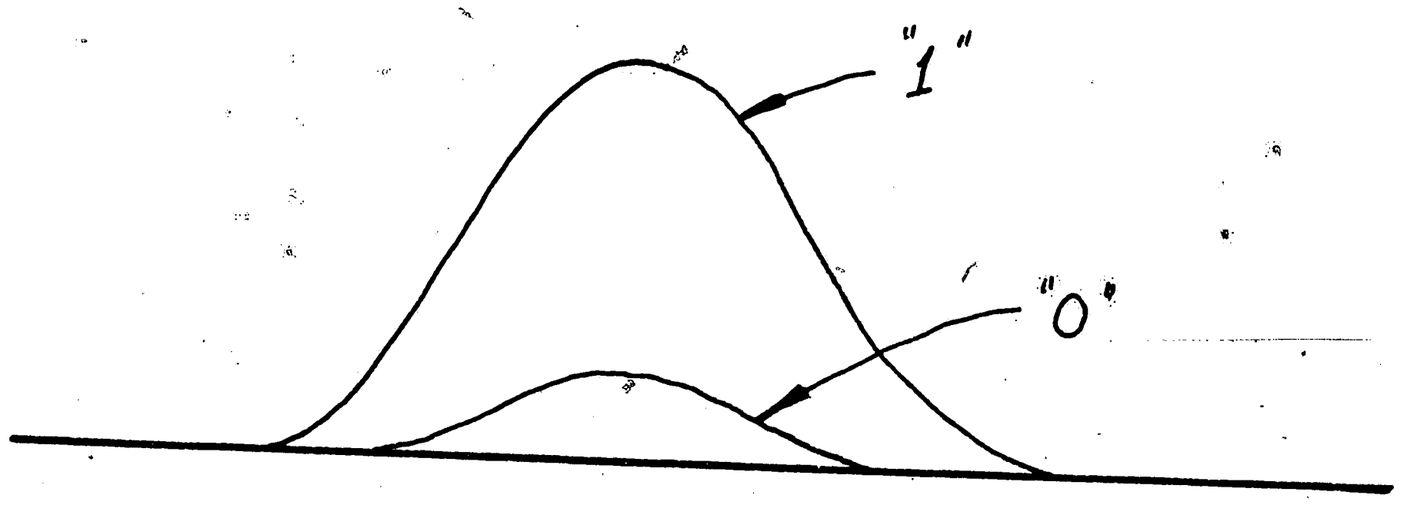

FIG. 10 - READ - SENSE OUTPUTS

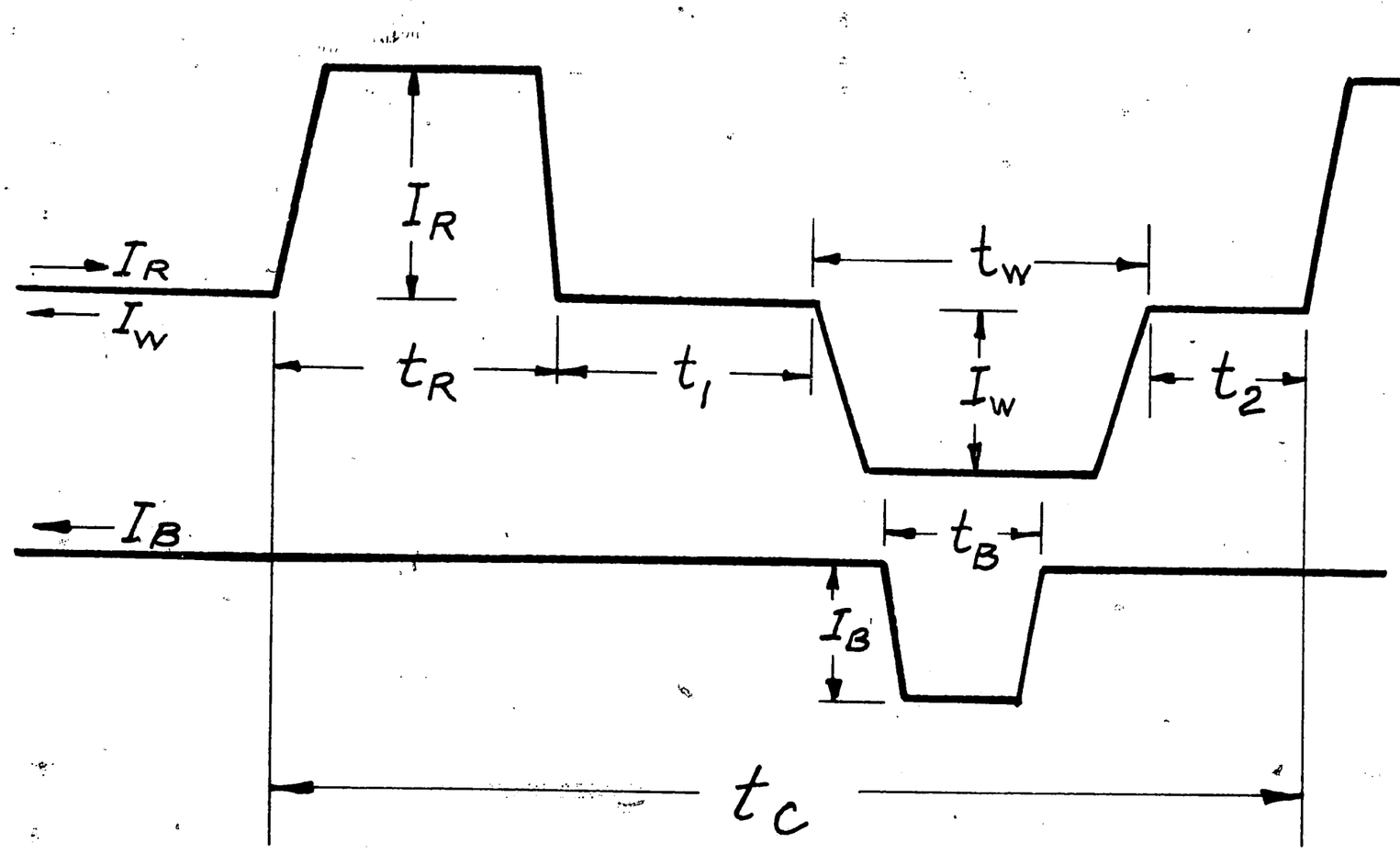

FIG. 11 - CYCLE TIME OF 2D MEMORY SCHEME

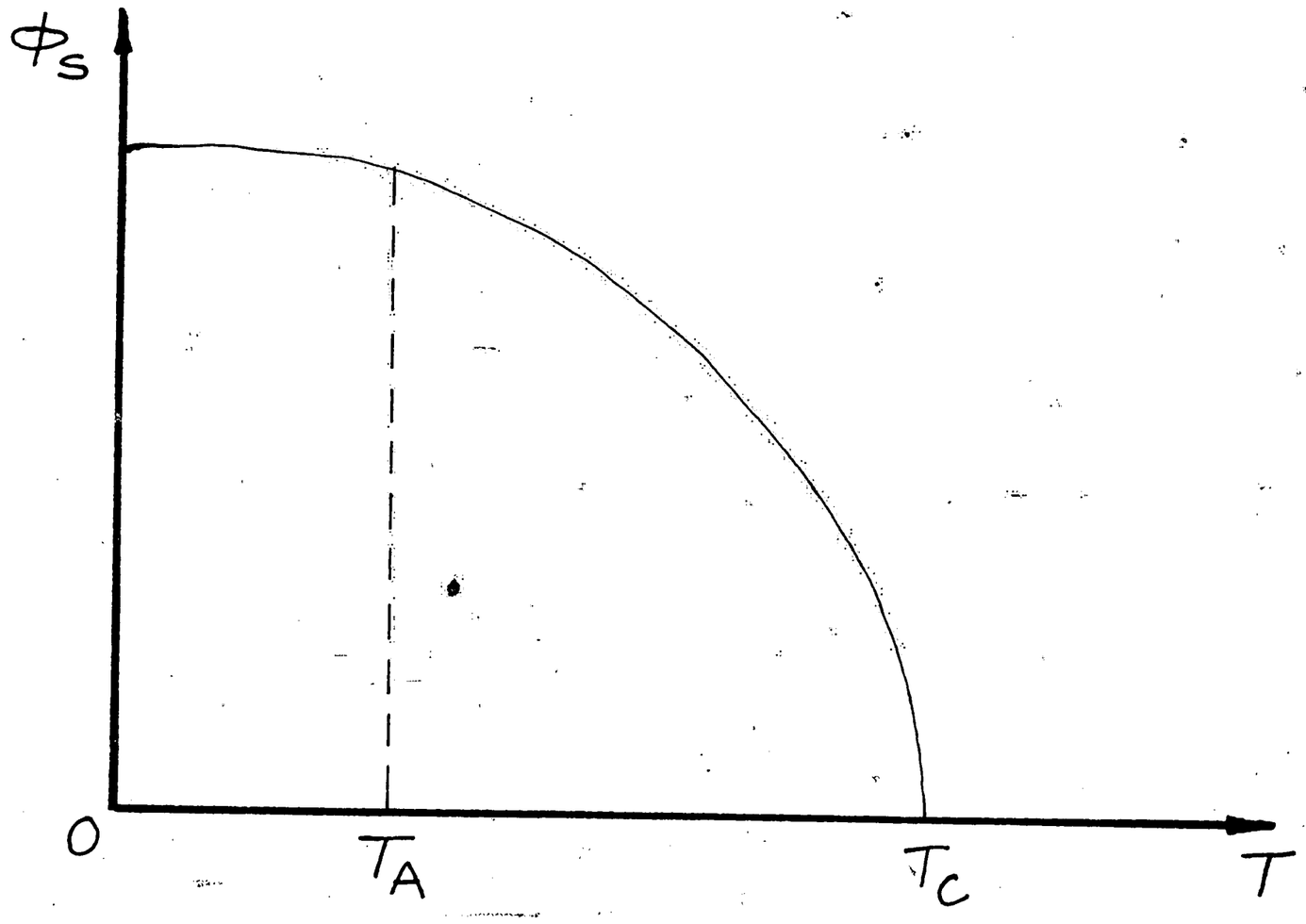

FIG. 12 - TEMPERATURE DEPENDENCE OF SATURATION FLUX
T_C = CURIE TEMP., T_A = AMBIENT TEMP.

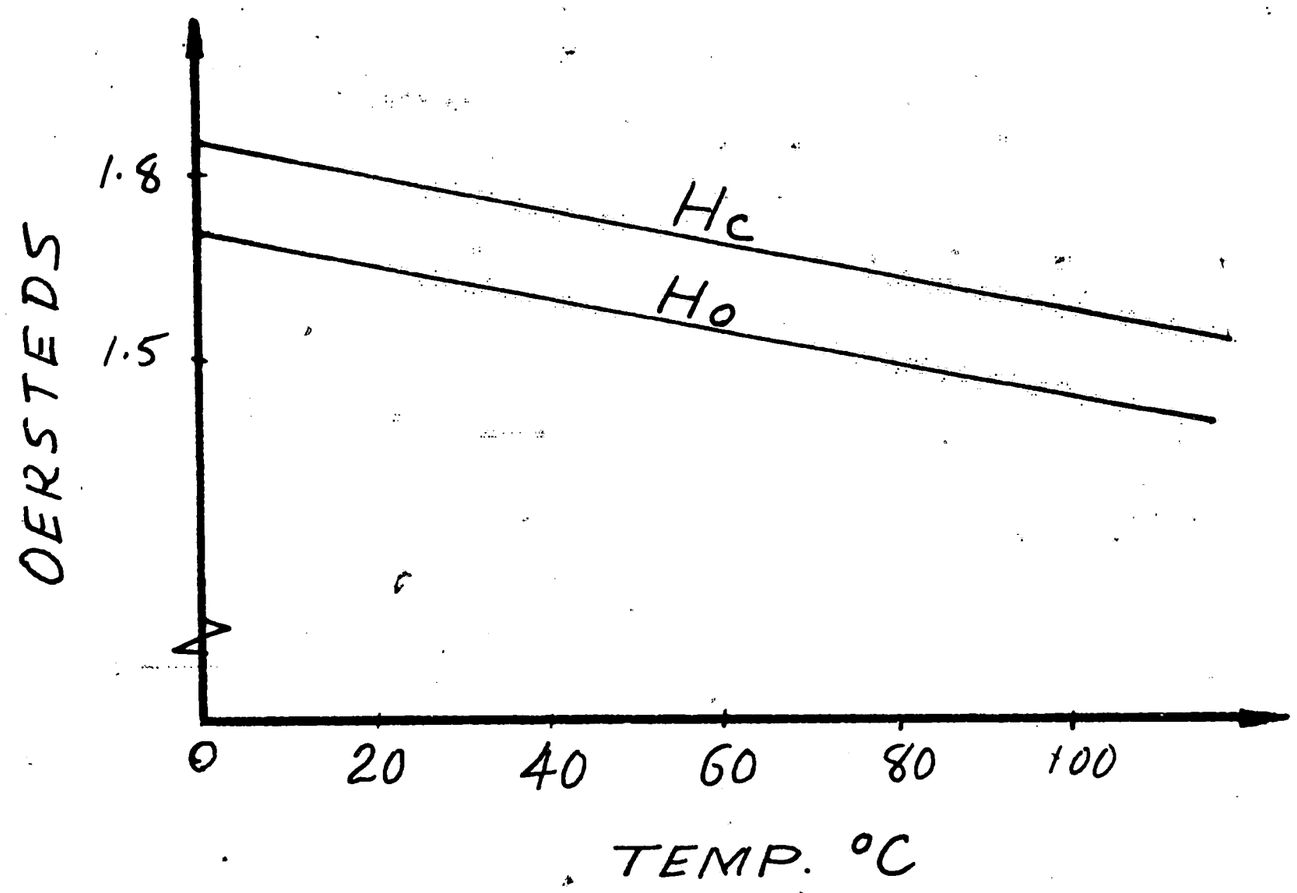

FIG. 13 - VARIATION OF H_c AND H_o WITH TEMPERATURE (DATA TAKEN OR INFERRED FROM REF. 16)

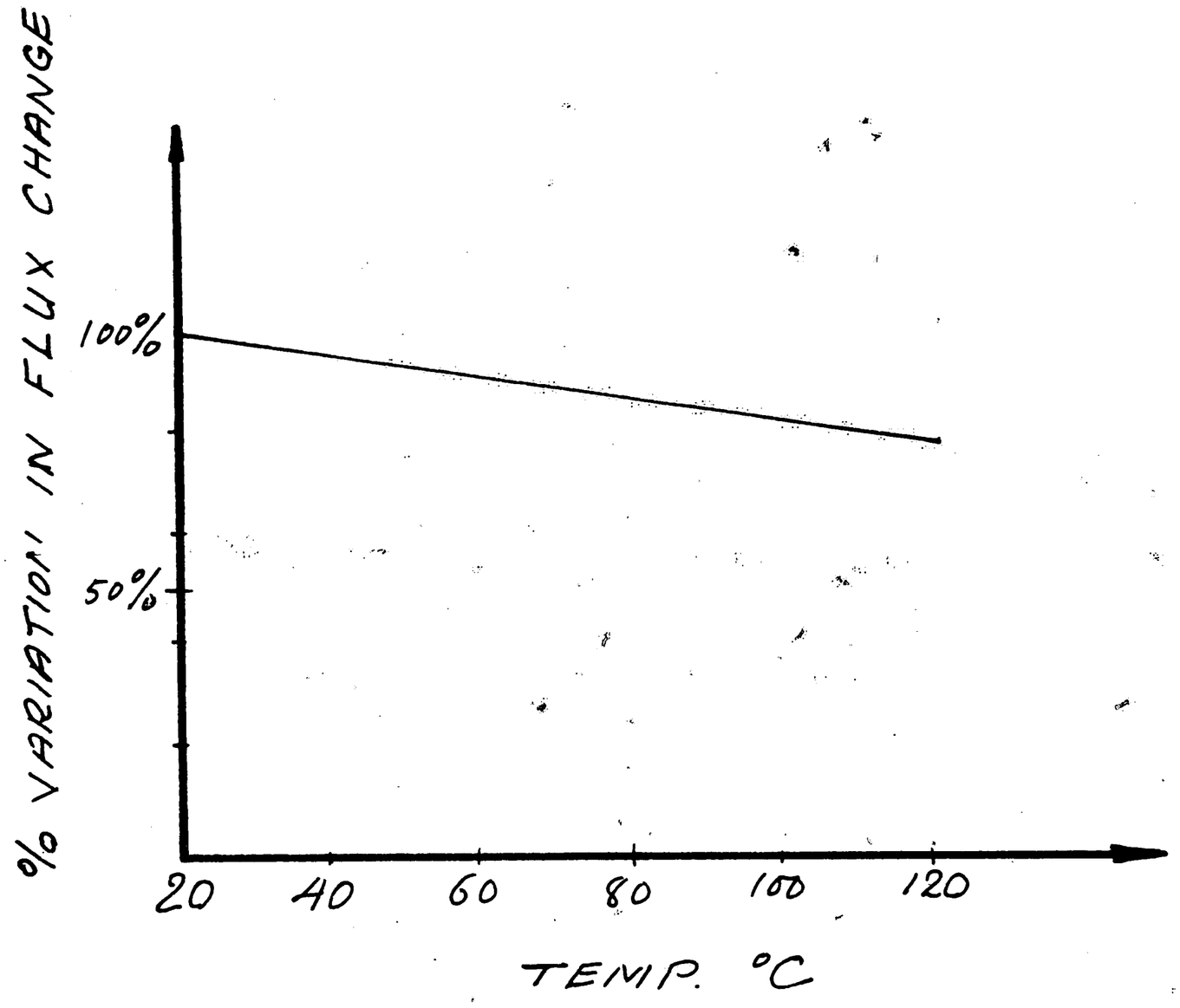

FIG. 14. PERCENT VARIATION OF FLUX CHANGE WITH TEMPERATURE

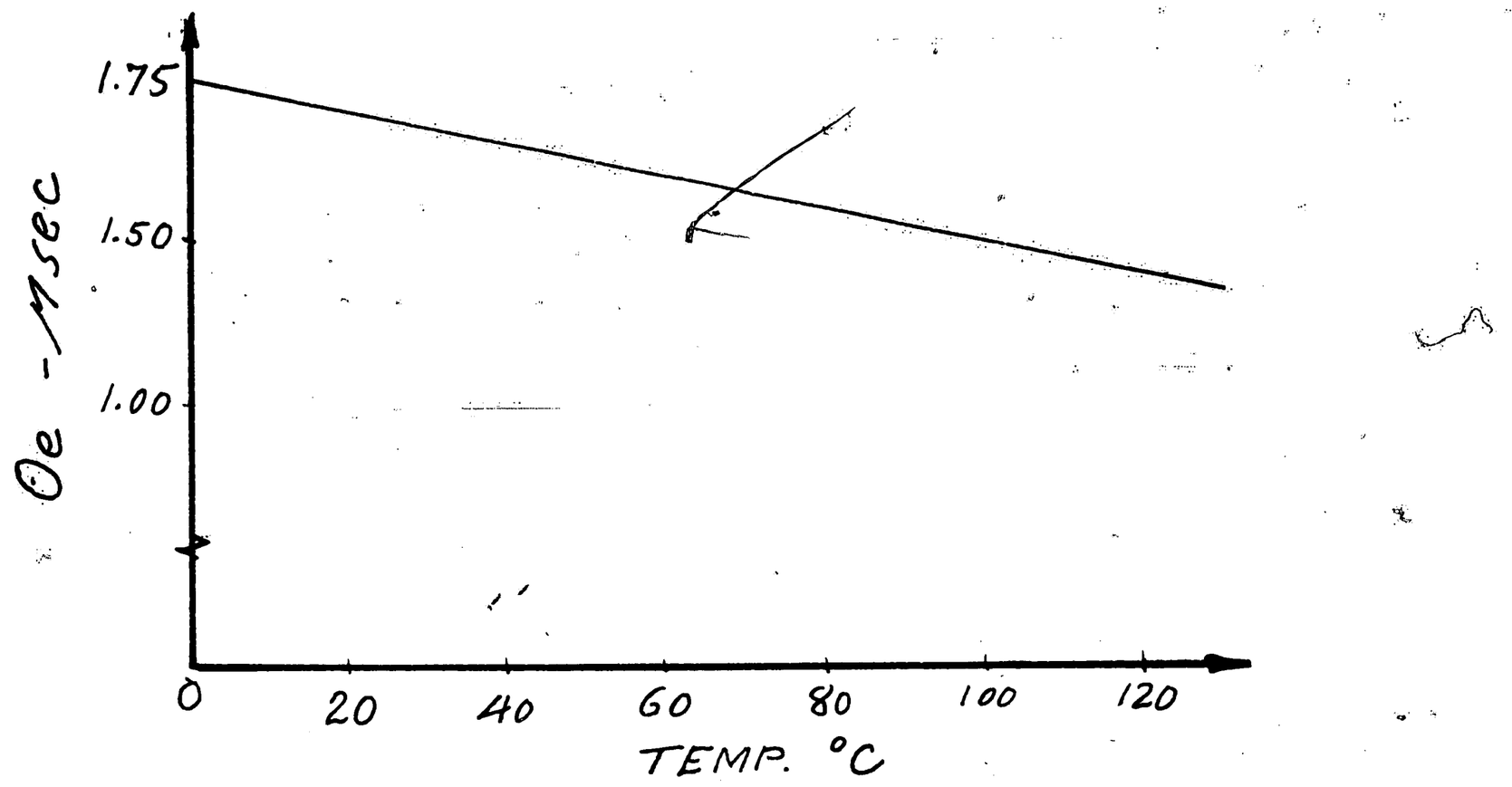

FIG 15 - VARIATION OF SWITCHING COEFFICIENT, S_o, WITH TEMPERATURE (DATA TAKEN FROM REF. 16)

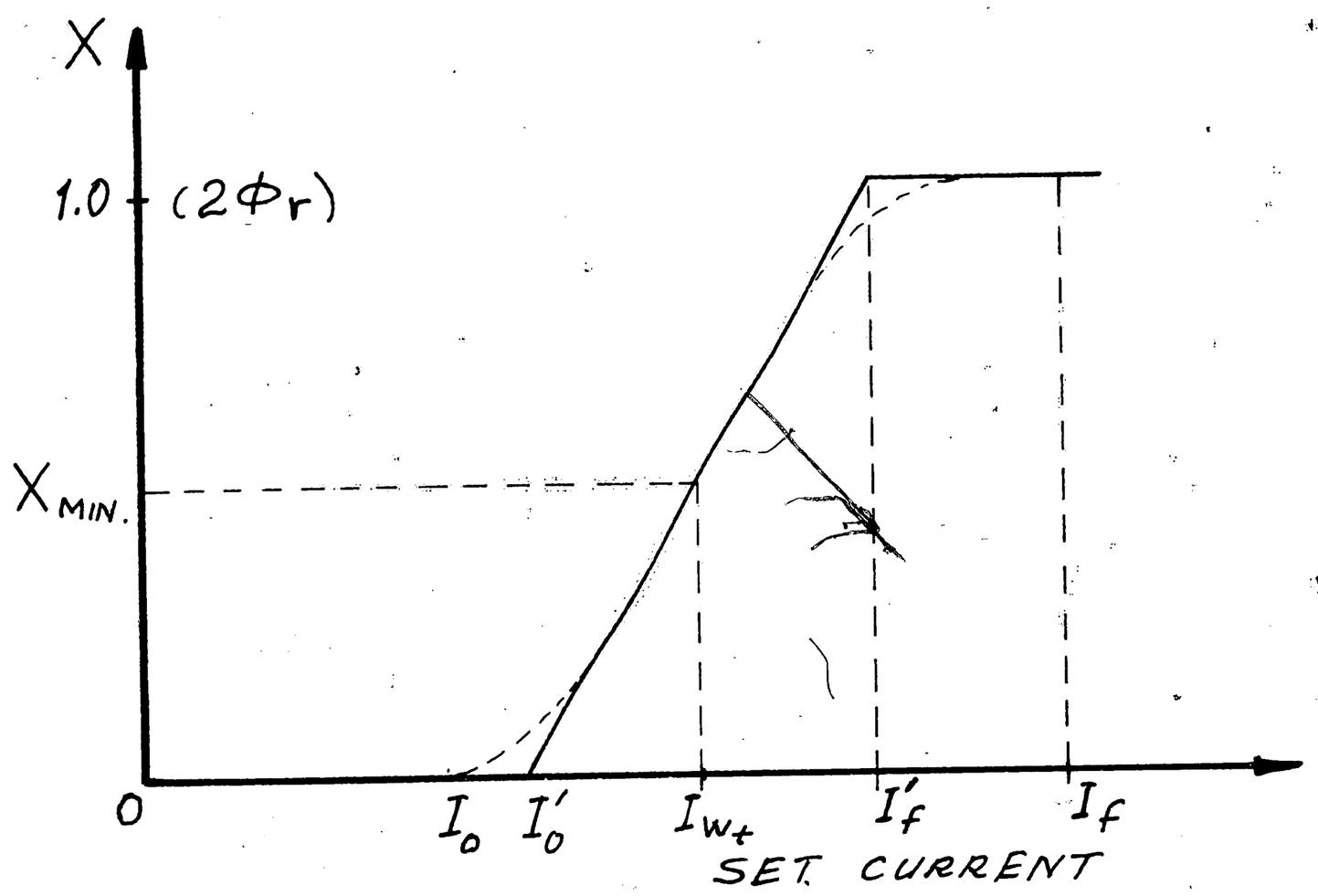

FIG. 16 - LINEARIZED "S" CURVE

References

1. Bozorth, R. M. Ferromagnetism. New York: D. Van Nostrand Co., 1951.

2. Chikazumi, S. Physics of Magnetism. New York: John Wiley & Sons, Inc., 1964.

3. Meyerhoff, A. J. Digital Applications of Magnetic Devices. New York: J. Wiley & Sons, Inc., 1960.

4. Edwards, D. B., et al. "Ferrite-Core Memory Systems with Rapid Cycle-Time, "Proc. IEE, Vol. 107B (1960), p. 585.

5. Menyuk, N., and Goodenough, J. B. "Magnetic Material for Digital Computer Components-I. A Theory of Flux Reversal in Polycrystal Ferromagnetics," J. Appl. Phys., Vol. 26 (1955), p. 8.

6. Shevel, W. L., "Observations of Rotational Switching in Ferrites," IBM J. Res. Developm., January, 1959, p. 93.

7. Stevens, M. C. "Ferrite Core Parameter Measurements at Very High Switching Currents," Electronic Engineering, Vol. 36 (1964), p. 470.

8. Stuart-Williams, R. "An Evaluation of Partial-Switching in Storage Applications," Solid State J., Vol. 2, No. 11 (1961), p. 25.

9. Tancrell, R. H., and McMahon, R.E. "Studies in Partial Switching of Ferrite Cores," J. Appl. Phys., Vol. 31 (1960), p. 762.

10. Shevel, W.L., and Chang, H. "A New Approach to High-Speed Storage-Low Flux Density Materials," J. Appl. Phys., Vol. 31 (1960), p. 1255.

11. Simkins, Q. W. "The State of the Art of Magnetic Memories," J. Appl. Phys., Vol. 33 (1962), p. 1020.

12. Edwards, D. B. J., et al. "High-Speed Ferrite-Core Storage System," Proc. IEE, Vol, 111 (1964), p. 1501.

13. Ref. 4, p. 586.

14. Ref. 8, p. 26.

15. Ref. 12, p. 1508.

16. Im, I. B., and Wickham, D. 6. "Square-Loop Properties of Materials" J. Appl. Phys., Vol. 35 (1964), p. 1442.

17. Shahan, V. T., and Gutwin, O. A. "Threshold Properties of Partially Switched Ferrite Cores," J. Appl. Phys., Vol. 33 (1962), p. 1049.

18. Holzinger, C. S. "Technique for Determining the Speed Capabilities of 2D Ferrite Core Memories," IEEE Transactions on Magnetics, Vol. 1, No. 4, (1965), p. 315.

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